# Werner Haas <br> Design Engineer 

Intel Labs, Braunschweig (Germany)

## SYSTEM-LEVEL IMPLICATIONS OF NON-VOLATILE, RANDOM-ACCESS MEMORY

## Level-Setting

- Intel Labs
$\rightarrow$ No conclusions on future roadmap possible
$\rightarrow$ No disclosure of research details
- Electrical engineer
$\rightarrow$ No new computer architecture concepts
$\Rightarrow$ No low-level material science
o System-level implications
$\Rightarrow$ No direct link to Barrelfish


## Can Barrelfish provide a

 better environment for experimentation?
## Emerging Memory Technologies

(1)

- "Computer memory innovation is nearly irresistible" (R\&D Magazine, Oct. 11)
- Charge-based memories (DRAM, Flash) face severe scalability problems
- Industry-focus on resistance as information carrier
o Implicit non-volatile storage $\rightleftharpoons$ NVRAM
o Opportunity for universal memory (working memory and storage)


## Emerging Memory Technologies

(2)
o Current prototypes

- PCM

Phase-Change Memory

- STTRAM
- ReRAM Resistive RAM

| Technology | DRAM | PCM | STTRAM | ReRAM |
| :--- | :---: | :---: | :---: | :---: |
| Density | 0 | + | - | ++ |
| Latency (ns) | $10 / 10$ | $20 / 50$ | $6 / 12$ | $10 / 10$ |
| Energy (pJ/b) | 2 | 100 | 3 | 2 |
| Endurance | $\mathrm{n} / \mathrm{a}$ | 10 e 8 | 10 e 15 | 10 e 12 |

[^0]
## System Implications

○ DRAM $\rightarrow$ NVRAM

- But volatile memory in cache hierarchy
- SW-transparent vs. SW-managed
- Virtual memory
- Huge physical address space
- Protection of storage-class data
o Persistent memory
- Orthogonal persistence
- صate anoniritm

Can Barrelfish provide a
better environment for experimentation?


[^0]:    Taciano Perez, Cesar A.F. De Rose:
    Non-Volatile Memory: Emerging Technologies And Their Impacts on Memory Systems

